IN THE SPECIFICATION

Please replace the paragraph at page 13, lines 3-4, with the following rewritten paragraph:

~~unit transistors which generate the programming current in the source driver circuit are n-channel transistors,~~ and

Please replace the paragraph at page 113, lines 14-25, with the following rewritten paragraph:

Incidentally, although it has been stated in the above example that pixel rows are scanned one by one, the present invention is not limited to this. For example, in the case of interlaced scanning, pixel rows are scanned skipping one pixel row. That is, even-numbered pixel rows are scanned in the first ~~frame~~ field. Odd-numbered pixel rows are scanned in the second ~~frame~~ field. When the first ~~frame~~ field is being rewritten, the images written into the second ~~frame~~ field are retained. However, blinking is caused (or may not be caused). When the second ~~frame~~ field is being rewritten, the images written into the first ~~frame~~ field are retained. Of course, blinking may be caused as in the example of Figure 174.

Please replace the paragraph at page 114, lines 1-16, with the following rewritten paragraph:

In the case of interlaced scanning, one ~~field~~ frame consists of two ~~frames~~ fields, which is normally the case with CRTs. However, the present invention is not limited to this. For example, one ~~field~~ frame may consist of four ~~frames~~ fields. In that case, images in the (4N + 1)-th pixel rows are rewritten in the first ~~frame~~ field (where n is an integer not smaller than 1). Images in the (4N + 2)-th pixel rows are rewritten in the second ~~frame~~ field. Images in the (4N + 3)-th pixel rows are rewritten in the third ~~frame~~ field. Images in the (4N + 4)-th

pixel rows are rewritten in the final fourth ~~frame~~ field. Thus, writing into pixel rows according to the present invention is not limited to sequential scanning. The above items also apply to other examples. The interlaced scanning as referred to herein means typical skip scanning and is not limited to "2 ~~frames~~ fields = 1 ~~field~~ frame." That is, one ~~field~~ frame may consist of a plurality of ~~frames~~ fields.

Please replace the paragraphs beginning at page 116, line 19, through page 118, line 14, with the following rewritten paragraphs:

In Figure 179, it is assumed for ease of explanation, that the screen is made up of four display periods (a), (b), (c), and (d). It is also assumed that one ~~field~~ frame consists of four ~~frames~~ fields with Figure 179(a) corresponding to the first ~~frame~~ field, Figure 179(b) corresponding to the second ~~frame~~ field, Figure 179(c) corresponding to the third ~~frame~~ field, and Figure 179(d) corresponding to the fourth ~~frame~~ field. In Figure 179, the display repeats a cycle of (a) → (b) → (c) → (d).

In the first ~~frame~~ field, the even-numbered pixel rows are selected in sequence to rewrite images as illustrated in Figure 179(a). When the first ~~frame~~ field is rewritten, the screen 50 is filled with black display in sequence from the top as illustrated in Figure 179(b) (Figure 179(b) shows the screen 50 filled with black display). Next, in the third ~~frame~~ field, images are written into the odd-numbered pixel rows in sequence from the top of the screen 50 as illustrated in Figure 179 (c). In other words, odd-numbered images are displayed in sequence from the top. Next, in the fourth ~~frame~~ field, images are put into non-illumination mode (black display) in sequence from the top of the screen 50 (Figure 179(d) shows the screen 50 completely in non-illumination mode).

Incidentally, the words "images are written" and "images are displayed" are used in Figures 179 (a) and (c), and basically the present invention is characterized in that images are

displayed (illuminated). Thus, writing an image (running a program) does not need to be identical with displaying an image. That is, one may think that in Figures 179(a) and (c), by controlling the gate signal lines 17b, the present invention controls the current flowing through the EL elements 15, and thereby puts images into illumination or non-illumination mode. Thus, it is possible to switch between the state in Figure 179(a) and state in Figure 179(b) at once (e.g., in a period of 1 H). For example, this can be done through control of an enable terminal (on-state and off-state are held in the shift registers of the gate driver circuit 12b (in Figure 179(a), the shift register for the even-numbered pixel rows holds on-state data) and the states in Figures 179 (b) and (d) are displayed when the enable terminal is off and the state in Figure 179(a) is displayed when the enable terminal is on). Thus, the displays in Figures 179(a) and 179(c) can be achieved using on-state and off-state of the gate signal lines 17b (image data is held in the capacitor 19 beforehand in the case of the pixel configuration in Figure 1, for example). It has been stated that each of the modes in Figures 179(a), (b), (c), and (d) occurs for one ~~1 frame~~ field period.

Please replace the paragraph beginning at page 119, line 21, through page 121, line 4, with the following rewritten paragraphs:

The drive system in the example of Figure 179 involves displaying images in the odd-numbered pixel rows or even-numbered pixel rows in the first and third ~~frames~~ fields and inserting a black screen (Figures 179(b) and (d)) between the two screens. However, the present invention is not limited to this. The display mode in Figure 168 may be brought about in the first and third ~~frame~~ fields and black display may be inserted between the two ~~frames~~ fields.

A timing chart for an example described below is shown in Figure 180. Figure 180(a) corresponds to the first ~~frame~~ field and Figure 180(b) corresponds to the second ~~frame~~ field

which is in black insertion mode. Figure 180(c) corresponds to the third ~~frame~~ field. Incidentally, the fourth ~~frame~~ field, which is the same as that in Figure 180(b), has been omitted. However, the fourth ~~frame~~ field is not strictly necessary. One ~~field~~ frame may consist of three ~~frames~~ fields. Since black screen is inserted in the second ~~frame~~ field, blurred moving pictures are reduced greatly. Thus, in Figure 180, a cycle of (a) → (b) → (c) is repeated.

In Figure 180(a), images are displayed in Figure 168(a) for 1 H in every four horizontal scanning periods (4 Hs) (a Vgl voltage (turn-on voltage) is applied to each gate signal line 17b for 1 H in every 4 Hs). Next, in the second ~~frame~~ field, a turn-off voltage (Vgh) is applied to all the gate signal lines 17b. This can be done at once through control of the enable terminal as is the case with the previous example. Thus, it is not strictly necessary to maintain the state in Figure 180(b) for one ~~frame~~ field period. To achieve proper movie display, it is enough to maintain the state for 4 msec or longer. However, in Figure 180(a), if images are rewritten in sequence from the top of the screen (not necessarily from the top), images will be skipped. The state in Figure 180(b) can be maintained easily by connecting the plural gate signal lines 17b in the lump and controlling the enable terminal as described with reference to Figure 179.

Please replace the paragraph at page 122, lines 10-24, with the following rewritten paragraph:

In the above example, the same turn-on/turn-off voltage patterns are applied to the gate signal lines 17b in each frame (unit period). However, according to the present invention, different pixel rows (pixels) are illuminated (display) or non-illuminated (non-display) for approximately equal durations during a predetermined period. Thus, in the drive system, where one ~~field~~ frame consists of two ~~frames~~ fields, the signal waveforms applied to

the first ~~frame~~ field and second ~~frame~~ field may vary among different gate signal lines 17b. For example, a turn-on voltage may be applied to an arbitrary pixel row for a period of 10 Hs in the first ~~frame~~ field, and for a period of 20 Hs in the second ~~frame~~ field (in a unit period of two ~~frames~~ fields, a turn-on voltage is applied for a period of 10 Hs + 20 Hs). A turn-on voltage is also applied to the other pixel rows for a period of 30 Hs.

Please replace the paragraphs at page 123, lines 1-21, with the following rewritten paragraphs:

An example is shown in Figure 182. In Figure 182(a) (first ~~frame~~ field), a turn-on voltage is applied to the gate signal line 17b for each pixel row for one horizontal scanning period (1 H) in every four horizontal scanning periods (4 Hs). In Figure 182(b) (second ~~frame~~ field), a turn-on voltage is applied to the gate signal line 17 for each pixel row for 2Hs in every 4 Hs. Thus, in two ~~frames~~ fields, a turn-on voltage is applied for (1 + 2) Hs in every (4 + 4) Hs. However, in a unit period (two ~~frames~~ a fields in Figure 132), a turn-on voltage is applied to every gate signal line 17b for the same period. Thus, every pixel row is displayed at the same brightness (assuming a white raster display).

Incidentally, although it has been stated with reference to Figure 180 that a turn-on voltage is applied for 1 H in every 4 Hs, this is not restrictive. For example, a turn-on voltage may be applied for 1 H in every 8 Hs as illustrated in Figure 183. Also, in each ~~frame~~ field, signal waveforms may be applied to the gate signal lines 17b perfectly at random rather than periodically. It is sufficient if the total durations for which a turn-on voltage is applied during a unit period are equal among all the gate signal lines 17b.

Please replace the paragraph at page 325, lines 1-9, with the following rewritten paragraph:

A problem with the pixel configuration in Figure 1, Figure 38, or the like is that the amplitude of the gate signal line ~~12a~~ 17a causes changes to the electric charges in the capacitor 19, making it impossible to obtain predetermined gradations. Description will be given citing the pixel configuration in figure 1 for ease of explanation. Figure 138 illustrates changes in the potential of pixels 16 in the case of conventional current programming with the pixel configuration in Figure 1.